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ENGINEERING

A Hybrid Physical ASM-HEMT Model Using a Neural Network-Based Methodology

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Outline

- **Motivation**
- **Hybrid Physical Modeling**
- **Model Extraction Flow**
- **Model Validation**
- **Summary**

GaN Addresses High-Performance Needs

• **GaN HEMTs provide high Pout & PAE at mm-wave frequencies**

Properties of RF Semiconductors Properties of RF Semiconductors

Measurement vs. Physics-Based Models

- **Two prevalent modeling schemes at opposite ends of the spectrum**
- **Various trade-offs:** None satisfy a modeling engineer's ideal wish list \odot

Hybrid Physical Modeling Methodology

The Advanced SPICE Model for HEMTs

- **ASM-HEMT:** Surface-potential-based physical compact model
- **Model effectively captures a range of device non-idealities:**
	- Self-heating, mobility degradation, DIBL, velocity saturation, trapping, etc.

Model Limitations for C-V Characteristics

- **Problem:** ASM-HEMT fails to capture CV non-linearities of the device
	- Unable to fit measured CV curves using various approaches
- Most results in the literature only show fitting at one V_p bias point
	- Nonlinear behavior in HEMTs isn't modeled properly (in most models)

Modifying the Gate Charge Framework

- **Overlap capacitances are treated as constant capacitances**
- C_{gs}/C_{gd} formulation *insufficient* to model V_{DS}-dependent non-linearities
- **Hybrid:** We **compensate** for unmodeled nonlinear physical behavior by incorporating additional model parameters into ASM-HEMT framework

"Compensating" (Uses a Neural Network)

Implemented through Verilog-A

Modifying the Drain Charge Framework

- **Overlap capacitances are treated as constant capacitances**
- **C**_{ds} formulation **insufficient** to model V_{DS}-dependent non-linearities
- **Hybrid:** We **compensate** for unmodeled nonlinear physical behavior by incorporating additional model parameters into ASM-HEMT framework

Hybrid ASM-HEMT Drain Charge Formulation

Implemented through Verilog-A

$Q_{d,i}$ I_{ds} g_{ds} $|Q_{\sigma}$ Igd Igs C_{fr2} C_{fgd} C_{gso} R_{g2} gin $\begin{array}{c|c|c|c|c|c|c|c} \hline \end{array} \begin{array}{c} C_{\text{fgd}} & C_{\text{gso}} & C_{\text{fr2}} & C_{\text{fr2}} & C_{\text{fr2}} & C_{\text{dso}} & C_{\text{dso}} & C_{\text{fd}} & C_{\text{ds,NN}} & C_{\text{dsman}} \ \hline \end{array}$ Rds,ext $C_{\rm gso}$

R_{g1} σ_i C_{gdo} σ_i R_d $R_{gs,NN}$ R_{g1} g g Q_{g1} d $\mathsf{C}_{\mathsf{gdo}}$ C_{fr} $C_{\text{gd,NN}}$ R_{gd,NN} Intrinsic Device! G D Gate $\begin{bmatrix} L_g & i \\ 0 & 0 \end{bmatrix}$ $\begin{bmatrix} R_{gs,NN} & R_{g1} \\ R_{gg} & i \end{bmatrix}$ $\begin{bmatrix} R_d \\ R_d \\ R_{g1} \end{bmatrix}$ di $\begin{bmatrix} R_d \\ R_d \\ R_{g1} \end{bmatrix}$ di $\begin{bmatrix} R_d \\ R_{g1} \\ R_{g1} \end{bmatrix}$ di $\begin{bmatrix} L_d \\ R_d \\ R_{g1} \end{bmatrix}$ di $\begin{bmatrix} L_d \\ R_{g1} \\ R_{g1} \end{bmatrix}$ L_d G

RGATEMOD = 1

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 R_g

 $\mathsf{C}_{\mathsf{gdo}}$ gi

Hybrid ASM-HEMT Model Equivalent Circuit

Cgdman

Lg

10/28/24 **BCICTS 2024 | OCTOBER 27-30, 2024 | FORT LAUDERDALE, FLORIDA, USA Slide 11** R_{s} S $\int_{\Gamma_{\text{decay}}}$ C_{dsman} **O** Source Extrinsic Parasitic Elements Ls RGATEMOD = 2 $\mathsf{C}_{\mathsf{gso}}$ R_{g1} $\mathsf{C}_{\mathsf{gdo}}$ gi R_{g2} G

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Modeling a 150-nm GaN HEMT

- **High-performance GaN HEMT process on a SiC substrate**
	- Primarily targets 5G and mm-wave applications (Ku, Ka, Q-band)
- **Device Geometry:** $4x50 \mu m$ GaN HEMT ($L_G = 150 \text{ nm}$)

150 1400 W_{G} = 8x50 μ m \rfloor $\frac{2}{10}$ 125
 $\frac{1}{100}$ 100
 $\frac{1}{100}$ 75

50
 $\frac{1}{100}$ 25 1200 (mA/mm) $f = 100$ MHz $\sf f_{max}$ 1000 $W_G = 4x50 \mu m$ 800 $V_{D} = 20 V$ 600 $\overline{\mathsf{C}}$ 400 f_T 200 C 125 250 375 500 0 0 20 40 50 60 10 30 O I_D (mA/mm) $V_D(V)$ R. P. Martinez et al., *IEEE TMTT*, 2024.

DC Characteristics & NVNA Data Small-Signal Metrics

Extracting the ASM-HEMT DC Model

- Divide the parameter set into smaller subsets
- **2) Extract the DC model via derivative-free optimization (no manual efforts)**

Manual Extraction Flow

Extract V_{off} and subthreshold slope parameters for the low current region

Extract mobility and vertical field dependence parameters for the high current region

Fine-tune

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Evaluate Objective

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Run Sim.

Yes

HPO

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Perform train-test split

Set loss functions and ranges for model parameters

- **RF extraction package in IC-CAP 2) Extract the DC model via derivative-free optimization (no manual efforts)**
	- Reduce extraction time from weeks to hours!

Measurements Needed for Hybrid Model

• **Dataset used to extract model parameters in the hybrid model**

Nonlinear Junction Capacitances of 4x50 μm GaN HEMT

Obtaining Training Data for Hybrid Model

- **Goal:** Identify best model parameter value that aligns simulated results with measured device characteristics at each bias condition
- Logical sequence was established: $C_{GD} \rightarrow C_{GS} \rightarrow C_{DS}$

• **Minimize relative error at each bias using Levenberg-Marquardt:**

Neural Network Training for Hybrid Model

- **Neural network predicts hybrid model parameter at each bias**
	- Incorporated in Verilog-A model (replaces constant model parameter)
	- 6 hidden layers, 12 neurons each; Root Mean Square Error as loss function
- **Keysight's ANN Toolkit in IC-CAP is used to train neural network**

Neural Network Output for Hybrid Model

- **Extracted capacitance model parameters that minimize error between simulated and measured C-V characteristics**
- **Neural network output shows good agreement as a function of bias**

Baseline Model Fails to Model Capacitances

- **Baseline Model:** Unmodified model tailored to fit CV characteristics starting at $V_{DS} = 0$ V
- Unable to fit V_{DS}-dependence for all three CV curves (limited range)

Improved Fitting Using Hybrid Approach

- **Hybrid Model:** Incorporates "compensating" circuit elements to fit capacitances through a neural network (6 hidden layers, 12 neurons)
- Fitting of capacitances improved greatly as a function of V_G and V_D

Improved Fitting Using Hybrid Approach

- **Hybrid Model:** Incorporates "compensating" circuit elements to fit resistances through a neural network (6 hidden layers, 12 neurons)
- Fitting of resistances improved greatly as a function of V_G and V_D

S-parameter Model Validation

• **Mismatch between measured and simulated S-parameters**

– $V_D = 5 - 25$ V (ΔV_D = 5 V), V_G = -2.2 to -1 V (ΔV_G = 0.2 V), $I_D = 15 - 500$ mA/mm

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S-parameter Model Validation

• **Good agreement between measured and simulated S-parameters** – $V_D = 5 - 25$ V (ΔV_D = 5 V), V_G = -2.2 to -1 V (ΔV_G = 0.2 V), $I_D = 15 - 500$ mA/mm

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Set-up for Non-linear Validation

Large-Signal Non-linear Validation

- **Hybrid model accurately predicted gain compression and PAE**
- **Baseline model resulted in a poor fit for gain compression**
	- Baseline model confined to a $narrow$ V_{DS} range due to existing limitations

Dynamic Load-Line Validation

- **Dynamic load-lines accurately predicted by hybrid ASM-HEMT model**
- **Baseline model yields poor results due to poor fitting of capacitances**

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Summary

- **Introduced GaN technology and modeling schemes**
- **Evaluated strengths and limitations of measurement and physics-based models**
- **Proposed hybrid physical approach using ASM-HEMT model to improve fitting of capacitances and resistances**
- **Model validated against S-parameters, X-parameters, and dynamic load lines**

Code and detailed documentation to be available in IC-CAP 2025 to benefit the device modeling community